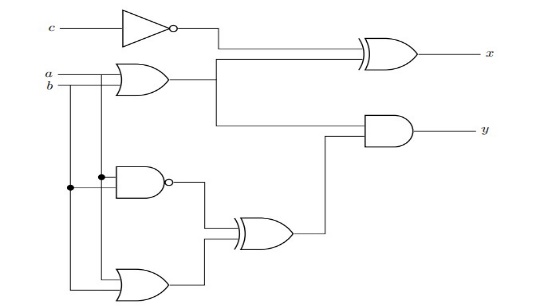
***Experiment 2: System Verilog Implementation***

System Verilog implementation involves creating a digital circuit using the System Verilog hardware description language (HDL). In simple terms, it means writing code to describe how the digital circuit should behave and how it's structured using System Verilog constructs.

**Circuit Diagram:**

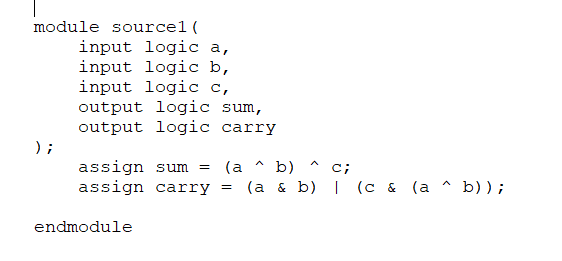
****

**Correction in code:**

**Source Code:**

The correction in this code are as follows:

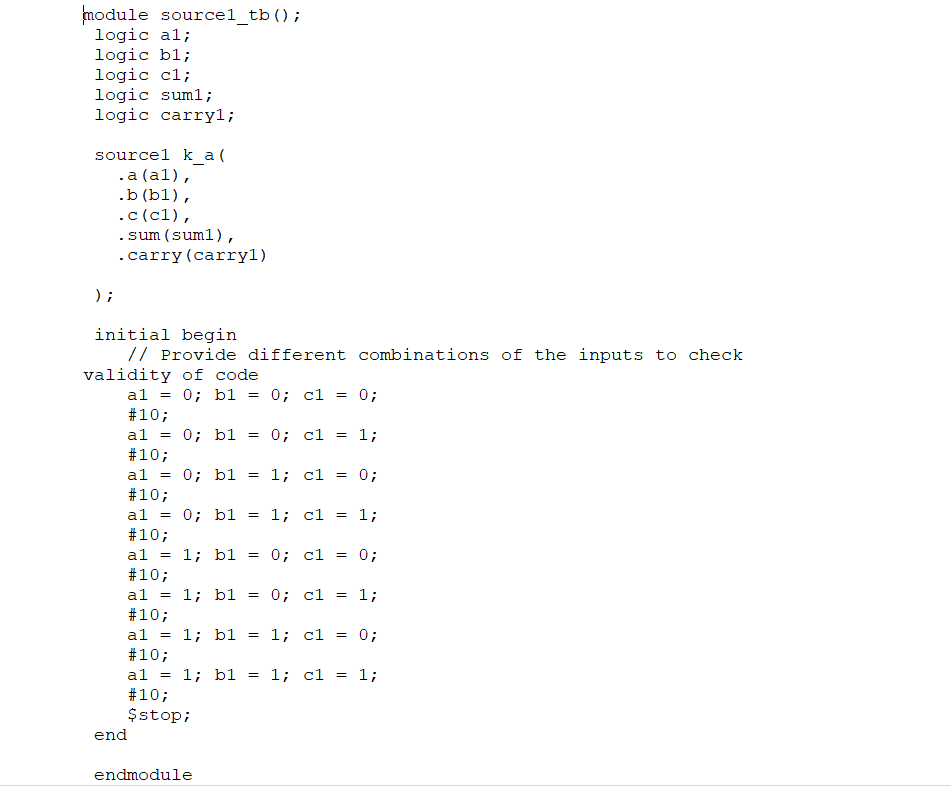
* In line no 7 there is no comma after logic carry
* In line no 10 the “&” operator is used after c



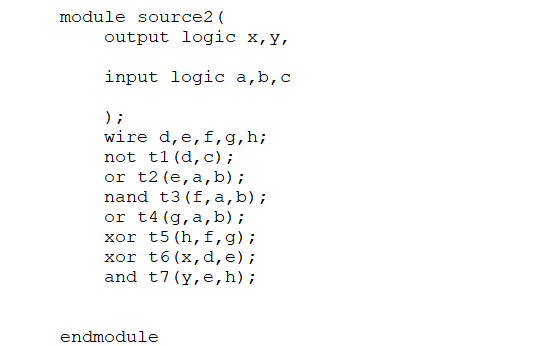
**Test Bench Code:**

The correction in the test bench code are as follows:

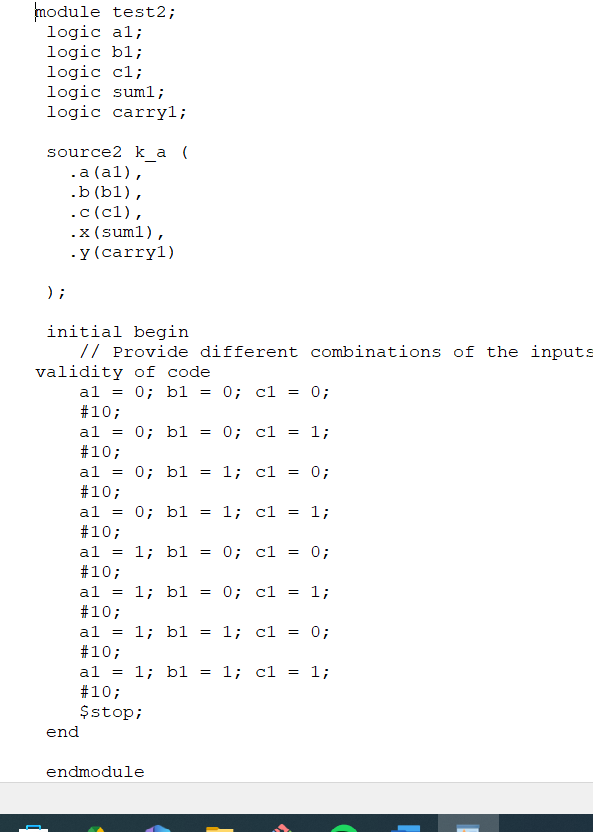
* In line 4 “**carry1**” is not declared anywhere in the test bench module
* In line 18,22,24,26,28,30,32 using variables **a1,b1,c1**
* In line 31 there is missing semicolon at the end of line
* In line 30,32 the variable a is used instead o**f a1**

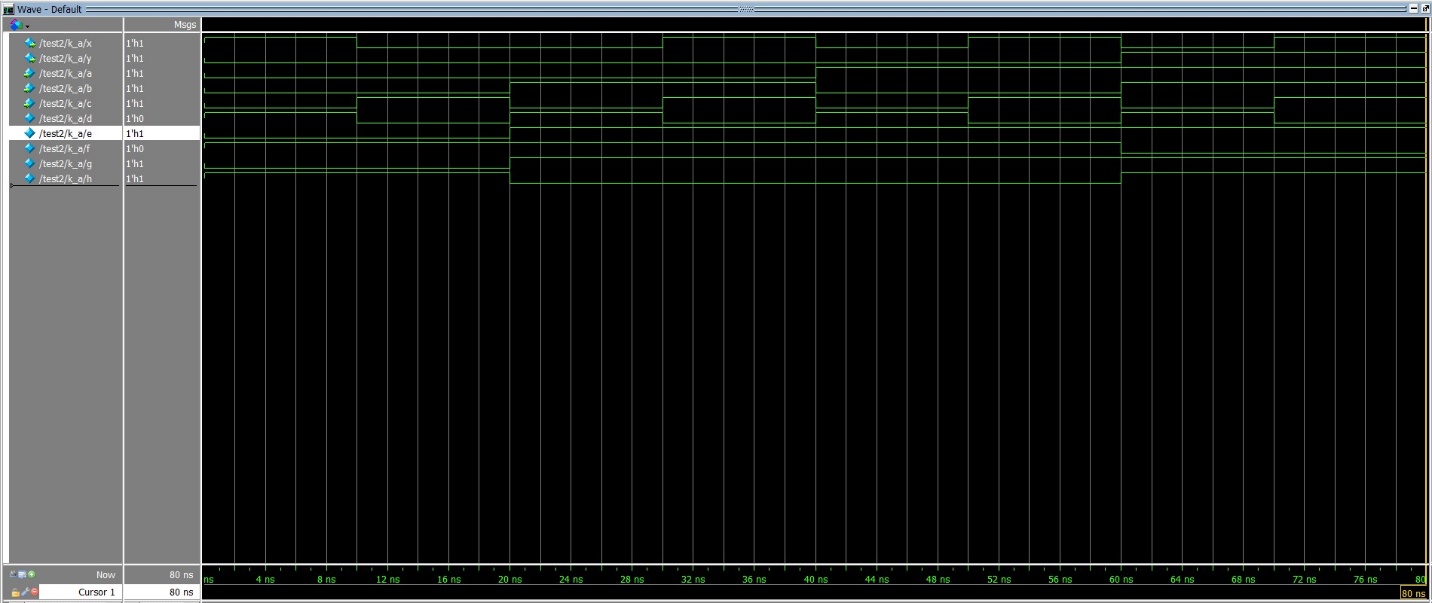


**System Verilog Codes of circuit and their graph:**

**Source code:**

**Test Bench Code:**

****

**Graph:**